DESCRIPTION

(Para 1) Background of the Invention

(Para 2) Field of the Invention

(Para 3) The present invention relates to the design of circuits used in communication systems, and more specifically to reducing the size of capacitors used in filters.

(Para 4) Related Art

(Para 5) Filters are used in various components. An example of such a component is a phase lock loop (PLL). As is well known, a PLL is generally used to generate an output signal, which is synchronized with an input signal. Often, the output signal is generated to have a frequency equaling a desired multiple ("frequency multiple") times the frequency of the input signal. PLLs find applications in several areas of communication (including long haul, short distance, wire-based and wireless), as is well known in the relevant arts.

(Para 6) In one prior embodiment, a PLL contains a phase detector (used synonymous with phase-frequency detector, for simplicity) which compares the phase of a divided (by the frequency multiple) output signal and the input signal (as a reference signal) in each comparison cycle. The phase of the output signal is adjusted according to the comparison such that the divided output signal is received in phase with the input signal.

(Para 7) A filter is often used to control such adjustments over multiple comparison cycles. The output of the filter indicates the extent to which the phase of the output signal is to be adjusted such that the output signal is generated with a desired phase/frequency. Thus, a filter may receive a signal indicating the phase error detected in a phase detector and generate another signal to adjust the phase of the output signal.

(Para 8) It may be desirable to provide filters with low bandwidth, generally for noise immunity (e.g., not to be affected by short term fluctuations due to reasons such as jitter and other types of noise) of the PLL loop. In one embodiment, the bandwidth of filter needs to be not more than 1/10 of the frequency of the input signal.

(Para 9) In one prior approach in which filters are implemented using capacitors, the value of the capacitors controls the bandwidth of the filter. The filter bandwidth can be designed to be low by choosing large capacitors. However, large capacitors are often difficult to fabricate as a part of integrated circuits. Such large capacitors may be provided as external components, but the corresponding implementations add to overall cost, require additional space/area, and also would be susceptible to more noise.

(Para 10) Accordingly, it is generally desirable that the size of such capacitors be minimized in PLL implementations.

(Para 11) Brief Description of the Drawings

(Para 12) The present invention will be described with reference to the following accompanying drawings.

(Para 13) Figure (Fig.) 1 is a block diagram of an example phase lock loop (PLL) in which several aspects of the present invention are implemented.

(Para 14) Figure 2 is a circuit diagram illustrating the details of a filter circuit in one prior embodiment.

(Para 15) Figure 3 is a circuit diagram illustrating the details of a filter circuit according to an aspect of the present invention.

(Para 16) Figure 4 is a block diagram illustrating an example device in which various aspects of the present invention can be implemented.

(Para 17) In the drawings, like reference numbers generally indicate identical, functionally similar, and/or structurally similar elements. The drawing in which an element first appears is indicated by the leftmost digit(s) in the corresponding reference number.

(Para 18) Detailed Description

(Para 19) 1. Overview

(Para 20) An aspect of the present invention enables a filter circuit of low bandwidth to be obtained by using capacitors of small sizes. In one embodiment, a passive component is connected between the input terminal and the output terminal of an operational amplifier. The input terminal is further connected to a combination of a first capacitor and a first resistor connected is series, with a second resistor being connected in parallel to the combination. In the case of a first order filter circuit, the

passive component contains a resistor, and in the case of a second order filter circuit, the passive component contains a capacitor.

(Para 21) Low bandwidth may be obtained for the filter by selecting appropriate values for resistors and capacitors. A small value of the capacitor can be made to be acceptable (i.e., to obtain desired transfer function) by increasing the resistance value of the second resistor. The noise due to the large resistor is attenuated by selecting a small value resistor for the first resistor.

(Para 22) As a result, low bandwidth filter circuits of acceptable noise can be realized using only small capacitors. The filter circuits thus designed can be incorporated into several components such as PLLs. Due to the use of small capacitors, such components can be fabricated as a part of an integrated circuit, thereby leading to advantages such as reduced cost/area requirement, and more noise immunity.

(Para 23) Several aspects of the invention are described below with reference to examples for illustration. It should be understood that numerous specific details, relationships, and methods are set forth to provide a full understanding of the invention. One skilled in the relevant art, however, will readily recognize that the invention can be practiced without one or more of the specific details, or with other methods, etc. In other instances, well-known structures or operations are not shown in detail to avoid obscuring the invention.

(Para 24) 2. PLL

(Para 25) Figure 1 is a block diagram of an example phase lock loop (PLL) in which various aspects of the present invention can be implemented. PLL 100 is shown containing phase frequency detector (PFD) 110, charge pump 120, filter circuit 130, voltage controlled oscillator (VCO) 150, and frequency divider 160. Each block is described below.

(Para 26) PFD 110 compares the phases of reference signal received on path 101 and feedback signal received on path 161, and generates an error signal on path 112 representing the difference in the phases of signals 101 and 161. Error signal 112 represents the phase error in the form of time signals, i.e., the path is asserted for a time duration proportionate to the phase error.

(Para 27) Charge pump 120 receives error signal 112 and converts the corresponding time signals into electric signals. The electric signals are provided on path 123. In one

embodiment described below, the electrical signals are provided in the form of voltage signals. PFD 110 and charge pump 120 are implemented in a known way.

(Para 28) Filter circuit 130 indicates on path 135 the extent (correction value, or signal) to which the phase of the output signal 159 should be adjusted by VCO 150. The correction value is determined by the transfer function of filter circuit 130, as well as magnitude of error signal 112. As noted above, filter circuit 130 may need to be implemented with a low bandwidth and without using large capacitors. The manner in which filter circuit 130 may be implemented according to various aspects of the present invention is described in sections below.

(Para 29) VCO 150 adjusts the frequency of output signal (having N-times the frequency of reference signal 101) provided on path 159 based on the correction value received on path 135. Since VCO 150 is controlled by voltage inputs, correction value 135 is received in the form of electric voltage. Feedback divider 160 divides the frequency of output signal 159 by N-times and provides the feedback signal on path 161.

(Para 30) Thus, the loop of VCO 15, feedback divider 160, PFD 110, charge pump 120, and filter circuit 130 adjusts the frequency/phase of output signal 159 until the phase error is substantially zero, in which case the steady state is said to have been reached.

(Para 31) As noted above, for loop stability the bandwidth of filter circuit (for low reference frequency & low jitter as mentioned earlier) 130 needs to be low. Various aspects of the present invention enable filter circuit 130 to be implemented with small capacitors. The advantages of the present invention may be appreciated in comparison to a prior circuit which does not employ one or more features of the present invention. Accordingly, the details of such a prior embodiment are described first below with reference to Figure 2.

(Para 32) 3. Prior Filter Circuit

(Para 33) Figure 2 is a circuit diagram illustrating the details of filter circuit 200 in one prior embodiment. Filter circuit 200 is shown containing resistor 210, and capacitors 220 and 230. Filter circuit 200 is shown receiving electric signal in the form of electric current, which is represented by current source 240. Each component is described below.

(Para 34) Resistor 210 and capacitor 220 together operate as a low pass filter to remove the noise components in the received electric signal. Capacitor 230 removes switching noise in the filtered signal and provides the filtered signal on path 299.

(Para 35) It may be noted that a pole and a zero are required to be present in the gain function of filter circuit for stability of a PLL. The pole is achieved with the operation of resistor 210 and capacitor 230, and the zero is achieved by the combination of resistor 210, and capacitors 220 and 230. Assuming that the resistance of resistor 210 equals R_2, and the capacitances of capacitors 230 and 220 respectively equal C_1 and C_2, the gain function (which is the impedance) of filter circuit 200, which contains both pole and zero is given by equation (1) below.

(Para 36) $G= ((1+T_2 s)*C0)/((1+T_1 s)*s)$ …….. Equation (1)

(Para 37) wherein s represents Laplace constant, $T_2 = R_2 C_2$,

(Para 38) *, + and / represent multiplication, addition and division operations,

(Para 39) $T1= R_2 (C_1 * C_2)/(C_1 + C_2)$ and

(Para 40) $C0= Iin/(2*pi)(C_1 + C_2)$, wherein Iin is the amount of current in the electric signal and pi is a constant equaling 22/7.

(Para 41) For a desired bandwidth (Wp) and a desired phase margin (phi) of a PLL, it can be shown that the maxima in the phase curve is obtained for the corresponding values of T_1 and Wp as given below with equations (2) and (3).

(Para 42) $T_1= (sec(phi) - tan (phi))/Wp$ …….. Equation(2)

(Para 43) $Wp= 1/sqrt (T_1 * T_2)$ …….. Equation(3)

(Para 44) wherein sec and tan are the trigonometric secant and tangent functions, and sqrt is square root.

(Para 45) Assuming that the gain of phase frequency detector and charge pump together is Kphi, and the gain of VCO is Kv, then the component values of filter circuit 200 are given below.

(Para 46) $C_1= ((T_1 Kphi\ Kv)/(T_2\ Wp^2\ N))\ sqrt((1+(Wp*T_1)^2)/(1+(Wp*T_2)^2))$ ……..Equation(4)

(Para 47) $C_2 = C_1 ((T2/T1)-1)$ …….. Equation(5)

(Para 48) $R_2 = T_2/C_2$ ……..Equation(6)

(Para 49) 4. Problem(s) with Prior Filter Circuit

(Para 50) As noted above, the bandwidth of filter circuit 130 generally needs to be low. One problem with such a requirement in prior filter circuit described above, is

that C_2 needs to be large for low bandwidth and better phase margin as may be observed from equations (2), (3) and (5) of above.

(Para 51) In one prior embodiment, such large capacitors are placed outside of integrated circuits, and is undesirable for reasons noted in the background section. Alternatively, the value of capacitor 220 can be decreased by increasing the value of resistor 210. An increase in R_2 causes a corresponding increase in noise.

(Para 52) A filter circuit according to various aspects of the present invention solves one or more of the problems as described below with reference to Figure 3.

(Para 53) 5. Filter Circuit

(Para 54) Figure 3 is a circuit diagram illustrating the details of a filter circuit according to an aspect of the present invention. For illustration, the details of the filter circuit is described with reference to Figure 1. However, the filter circuit can be implemented in other implementations as well. Filter circuit 130 is shown containing resistors 310 and 320, capacitors 330 and 340, and operational amplifier 350. Each component is described below.

(Para 55) Resistors 310, 320 and capacitor 330 together remove the noise components in the received electrical signal on path 123 and provide the filtered signal on inverting input terminal of operational amplifier 350.

(Para 56) Capacitor 340 operates to provide the desired gain of filter circuit 130, in addition to providing the pole at origin. Operational amplifier 350 amplifies the filtered signal and provides the amplified filtered signal on path 135 for further processing.

(Para 57) Assuming that the resistance of resistors 310 and 320 respectively equal R_A and R_B, and the capacitances of capacitors 330 and 340 respectively equal C_A and C_B, the gain function (G) of filter circuit 130, which contains both pole and zero is given by equation (7) (assuming that operational amplifier 350 is ideal) below:

(Para 58) $G= ((1+T_2 s)*C0)/((1+T_1 s)*s)$ ..... Equation (7)

(Para 59) wherein s is Laplace constant, $T_2 = (R_A + R_B) C_A$, $T1= R_A C_A$, $C0= Vin/(2*pi)(R_B C_B)$, Vin is the amount of voltage in the electric signal, and pi is a constant equaling 22/7.

(Para 60) For a desired bandwidth (Wp) and a desired phase margin (phi) of a PLL, the component values of filter circuit 130 are given by the equations below.

(Para 61) R_B= ((Kphi Kv)/(C_B Wp^2 N)) sqrt ((1+($Wp*T_2$)^2)/(1+($Wp*T_1$)^2)) .....Equation(8)

(Para 62) wherein sqrt represents the square root operation.

(Para 63) R_A= R_B/ ((T2/T1)-1) ..... Equation(9)

(Para 64) C_A = T_1/R_A ..... Equation(10)

(Para 65) It may be observed from the above equations that R_A and R_B depend on bandwidth Wp (and/or T2/T1), the value of C_B may be selected to set the value R_B, and C_A is independent of Wp.

(Para 66) From Equation (8) above, it may be appreciated that R_B needs to be high for a low bandwidth Wp. In general, large resistors are sources of noise. However, the noise due to high value of R_B would get attenuated due to the parallel connection of R_A. Thus, the noise at the output is (substantially) due to R_A only and the noise due to R_B is attenuated.

(Para 67) Therefore, with a high resistance value of resistor 320, the value of capacitor is reduced without increasing noise. Such a resistor with a high resistance can be easily integrated into integrated circuits (compared to large capacitors).

(Para 68) In one embodiment, assuming that a PLL is to be designed for Kv = 240e6 Hz/V, Kphi=100e-6 A, N=480/13, Wp= 100e3 * 2* pi rad/s, and Phi=60 * pi/180 rad, then the values of prior filter circuit 200 and filter circuit 130 are given below.

(Para 69) R1=1Kohms, C1=450pF, and C2= 5.2nF for prior filter circuit 200. However, RA=31Kohms, RB= 410Kohms, CA= 13pF, and CB= 150pF for filter circuit 130.

(Para 70) It may be noted that the C2 (of prior filter circuit 200) is a large value compared to C_B (of filter circuit 130). However, resistance value of R_B is high, and the noise caused by which is attenuated, as noted above.

(Para 71) It may be noted that structure of Figure 3 implements a second order filter. However, a first order filter circuit may be implemented by replacing capacitor 340 (passive component) with a resistor.

(Para 72) In addition, non-inverting terminal of operational amplifier is shown connected to ground and inverting terminal is shown connected to receive signal 123 through components 310, 320, and 330. However, non-inverting terminal of operational amplifier 350 can be connected to receive electric signal 123 and inverting terminal can be connected to ground through components 310, 320, and 330.

(Para 73) Furthermore, given that the non-inverting input terminal of Figure 3 is connected to ground, the approach of Figure 3 can be easily extended to differential implementations. In addition, filter circuit and PLL can be implemented in various devices. An example device is described below in further detail.

(Para 74) 6. Device

(Para 75) Figure 4 is a block diagram illustrating an example device in which various aspects of the present invention can be implemented. For conciseness, only the portions of device 400, as relevant to some aspects of the present invention are included. However, various aspects of the present invention can be implemented in other devices as well. Device 400 is shown containing PLL 100, analog to digital converter (ADC) 410 and processing block 450. Each block is described below in further detail.

(Para 76) PLL 100 receives generates a clock signal on path 159 based on an input signal received on path 101. ADC 410 samples an analog signal received on path 401 to generate digital values. Processing block 450 contains one or more processing units to process the digital values.

(Para 77) 7. Conclusion

(Para 78) While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. Thus, the breadth and scope of the present invention should not be limited by any of the above described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.